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Lab: Section 6

Digital Logic Final Project

Option #1: Increasing Numbers

Components used:

Register, Comparator, Seven Segment Decoder, Counter

Circuit Description and Explanations:

Register File (Figure 1):

For the register file, it takes in 1 bit at a time and enters it into the first DFF when the clock hits 1. After this any bits entered in, get moved down 1 DFF every time the clock pulses to 1. The output combines the first two bits and the last two bits into two, two-bit buses to only allow 2 read ports for the register file.

Comparator Circuit(Figure 2):

The comparator circuit takes in 4, 2-bit buses, which gets converted into 2, 4-bit numbers. I used XNOR gates to see if all the bits of the 2 numbers are equal, which will output 1 if that is true. Next, in order to find if A < B, we use ‘and’ gates with the A bit not’d. If A’ and B are both 1, since the MSB is the first bit compared, that would mean that A < B, and would output 1, since they end at a or gate. This goes on to compare each bit, with each A bit not’d, B, and if their equal from the first part.

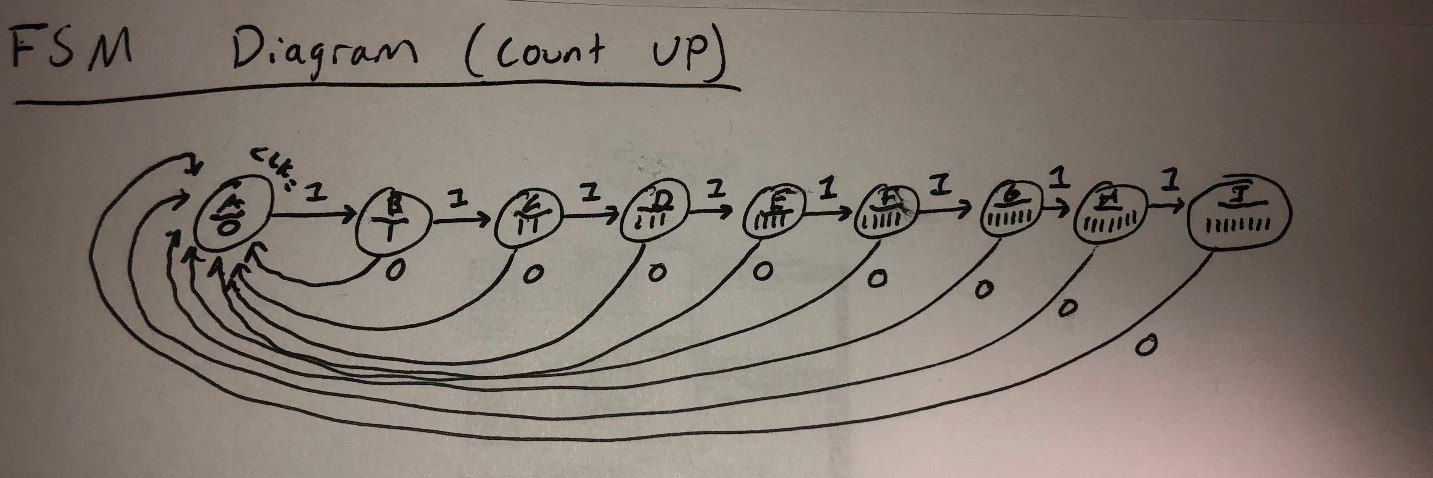
Increasing Number Order (Figure 3):

In this circuit, I take in numbers, one bit at a time and enter it into a register based on the register address given by switches on the board. The bit gets entered in one at a time, entering into the register every time the clock is pulsed. The clock uses a de-bouncer so that we could use a button for the clock without the pulse outputting irregular numbers. If you make a mistake, you can clear the register by selecting the correct register address and flipping the clear switch. Once you turn the mode into checking mode, you can no longer enter in numbers and the board will display if your numbers are in increasing order. If they’re not in increasing order, the board will light up a red LED at the address of the mistake.

The gates used out of the register blocks and on their input side, are their so you can only input numbers if you select the correct write address. The other gate is used for the same thing but for the clear option on each register.

The gates that are used to the right of the comparators are there so that if the mode is in the checking phase, it will only output the first error in the line of increasing numbers.

Counter (Figure 4.):

 For the FSM qualification needed for the project I used a machine that would iterate through 8 bits constantly making the next bit ‘1’ every clock cycle. I was able to use this to iterate through my output so that if one output was wrong, the rest of the output wouldn’t light up. I made this circuit by using 8 DFFS and setting the next one to 1 every clock cycle. There is also an enable input in this circuit that allows for the counter to be stopped and restarted.

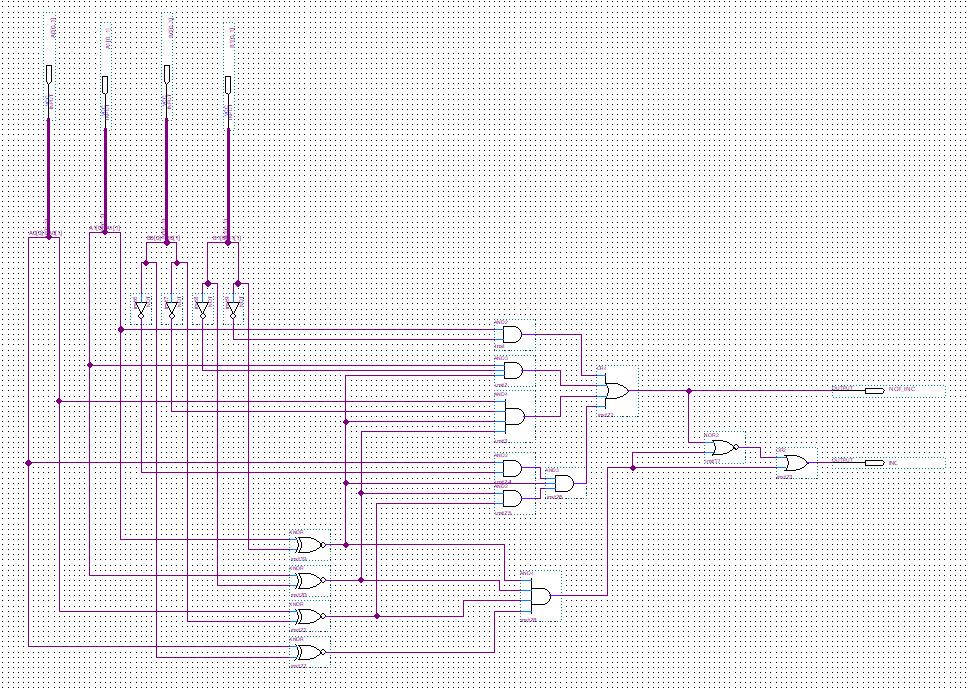
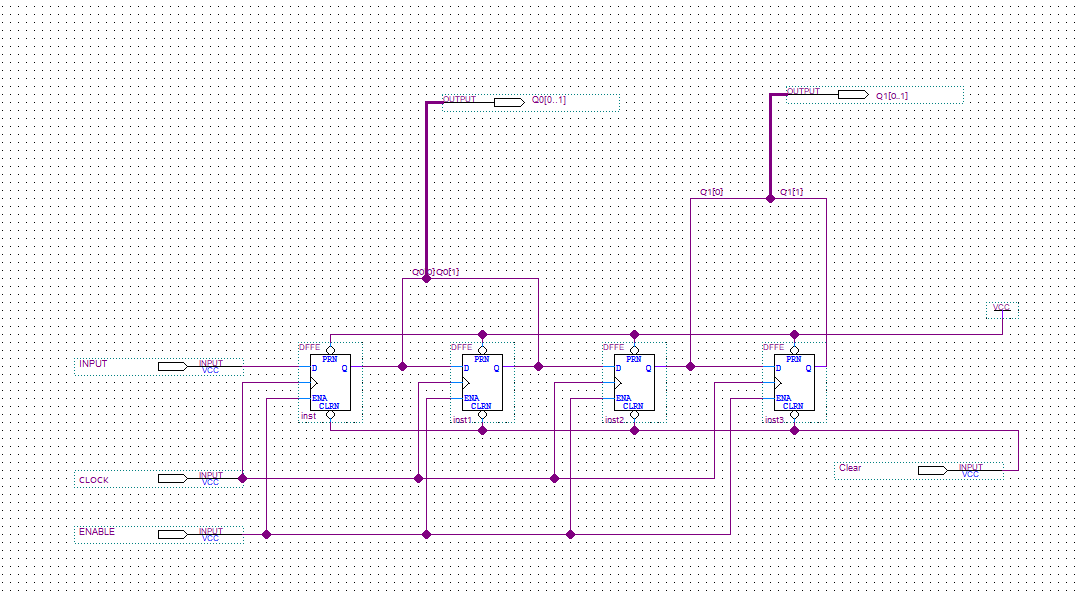
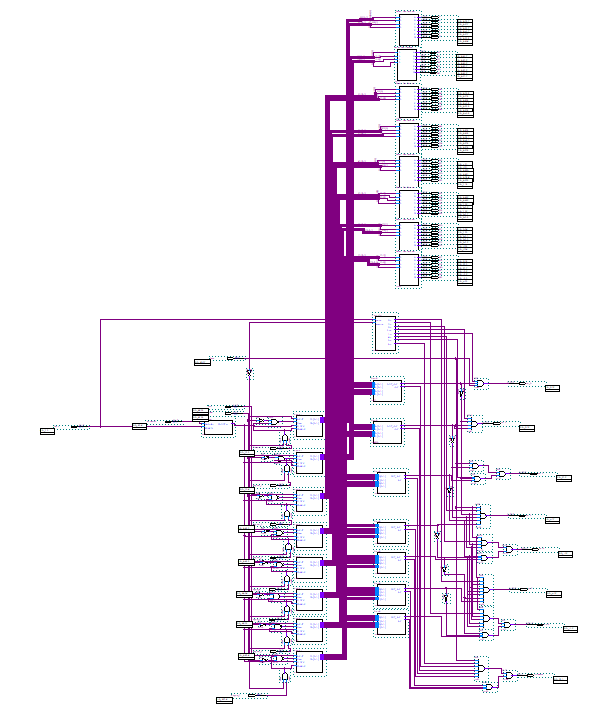
Figure 1.

Figure 2.

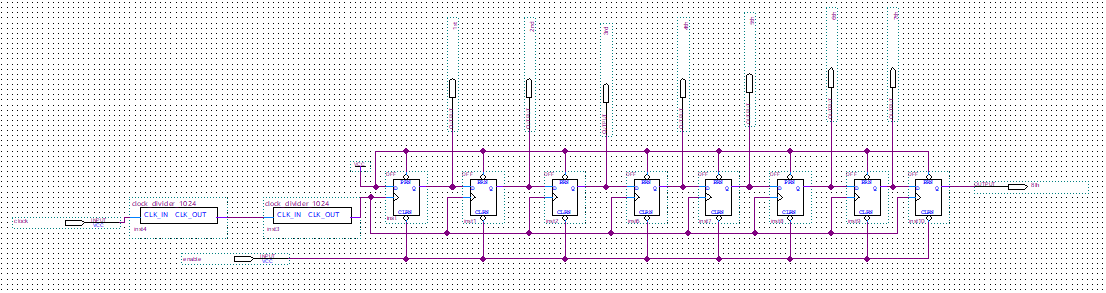
Figure 3.

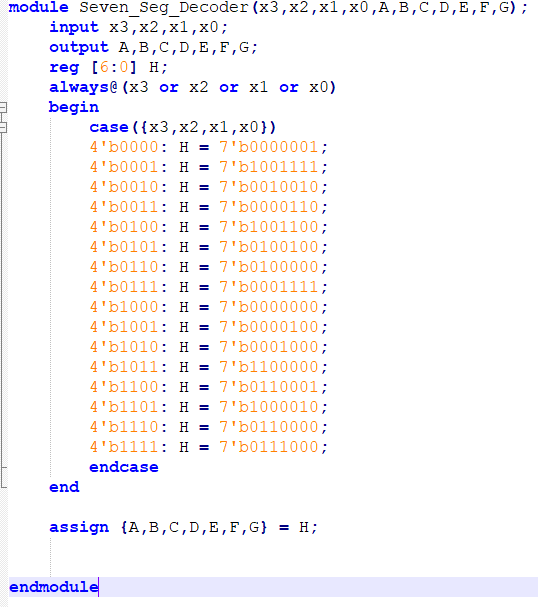
Counter (FSM)

Registers

Comparators

Seven Seg. Decoders



Figure 4. (above) Figure 5. (below)